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(54) FREQUENCY SYNTHESIZER WITH MULTIPLE CONTROL LOOPS

(71) We, ADRET ELECTRONIQUE, a French body corporate of Avenue Vladimir Komarov, 78190 Trappes, France, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention refers to the production of electric signals of variable frequency by means of techniques making use of the controlling of the frequency of an oscillator by comparing the said frequency with a standard frequency, the said comparison being effected in a known device called a phase detector or phase comparator.

A known frequency synthesizer comprises a first, phase-locking, control loop with a programmable frequency divider, a second, phase-locking, control loop without a programmable divider and without an analogical frequency approach system, means for inhibiting the second loop while the first effects a numerical approach to the frequency and for inhibiting the first loop and activating the second once this approach is completed, and another control loop which operates at the same time as the second and sets in motion the phase comparator of which it is comprised, this another or slave loop comprising also an amplifier for the output voltage of the phase comparator in the second loop, this amplifier being provided for the purpose of adjusting the said output voltage to the value zero.

Such an arrangement permits the generation, without appreciable phase noise, of a frequency PN, P being a predetermined frequency step and N a whole number programmable by means of the divider.

For certain applications it is necessary to generate a frequency $F = PN + \delta$, δ being a frequency increment which may itself comprise a fixed part F_0 and a variable part ϵ , positive or negative.

The known methods of obtaining such a result present considerable difficulties of real-

isation at high frequencies and are not capable of producing a frequency free from phase noise.

The invention consists in a generator of electric signals having a variable frequency comprising a main frequency and an increment, the said generator comprising a first oscillator which is controllable to generate the said main frequency, a first, phase-locking, control loop for the first oscillator, said first phase-locking loop being provided with a programmable frequency divider, a second, phase-locking, control loop for the first oscillator, comprising a phase comparator for receiving the output frequency of the first oscillator and harmonics of said main frequency, means for inhibiting the second loop while the first loop effects a numerical approach to the frequency of the first oscillator and for inhibiting the first loop, while activating the second loop, as soon as this approach is complete, a second oscillator, means for using a control voltage applied in the first loop to control the frequency of the first oscillator to impose on the second oscillator a frequency displaced from the output frequency of the first oscillator by an amount substantially equal to the increment, and a third, phase-locking, control loop for the second oscillator and comprising a phase comparator for receiving the increment and the difference in the output frequencies of the two oscillators. Thus, the frequency PN is generated by the first oscillator and the voltage which controls the frequency of this first oscillator is used to impose on the frequency of a second oscillator a value differing from the first by an amount roughly equal to the increment δ .

Thus a frequency approaching $PN + \delta$ is obtained at the second oscillator, the fine control of the frequency of this second oscillator being achieved by the phase-locking-loops.

Following a variation, the third, phase-locking, control loop may comprise a "phase-frequency" digital comparator followed by an integrator circuit.

The invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

5 Figure 1 represents the circuit of one form of a frequency synthesizer constructed in accordance with the invention;

Figure 2 represents an improved form of the synthesizer of figure 1 and

10 Figure 3 represents a modification of the synthesizer of Figure 2.

The synthesizer represented in figure 1 comprises a first oscillator 1 whose output frequency is applied to three separator devices 3a, 3b, 3c. These known devices prevent interaction between the different signals.

15 The separator 3b supplies a first frequency divider 5 with fixed ratio n , followed by a divider 6 with ratio N programmable by numerical control.

20 The output frequency of the divider 6 feeds a first phase comparator 7, which receives from another source a standard frequency P after division in the ratio n by a divider 8.

25 The output of the comparator 7 controls the frequency of the oscillator 1, for example by acting on the cathode of a variable capacity diode 1a. This control is effected through the intermediary of a field effect transistor 9 acting as an interrupter controlled by the output of a first coincidence device 10.

30 The device 10 is fed by the output signals of the dividers 6 and 8.

A condenser 13 connects the drain of the transistor 9 to earth.

35 The separator 3c feeds a second phase comparator 11 of the sampling type which receives a spectrum of harmonics of the frequency P in the form of short impulses, supplied by means of an appropriate circuit 12 of a known type.

40 The output of the comparator 11 is fed to the other electrode (the anode in the example shown) of the variable capacity diode 1a.

45 By way of a variation, the comparators 7 and 11 may act on two distinct variable capacity diodes, or on any other devices controlling the frequency of the oscillator 1.

50 An amplifier 14 having negative conductance (its output current $I_o = -GE$, G being the gain and E the input voltage) joins the output of the comparator 11 to the cathode of the diode 1a.

55 The part of the circuit which has just been described is known and comprises three controlling loops.

60 A first loop comprises the dividers 5 and 6 and the comparator 7. This loop is of the known type called "phase-locking". It permits the rapid locking of the oscillator 1 on to the desired frequency, without any risk of locking on to a harmonic of that frequency. This locking is achieved when the frequency F_1/nN issuing from the divider 6 is equal to

the frequency P/n issuing from the divider 8, that is to say when $F_1 = PN$. 55

As long as this first loop is not stabilised, the signal F_1/nN not being in phase with the reference impulses P/n , the negative peak of the signal F_1/nN coincides at certain instants with the reference impulses. The coincidence circuit 10 is used to activate the field effect transistor 9 during a predetermined time, so that the output signal issuing from the phase comparator 7 is transmitted to the diode 1a and the first loop is kept active. At the same time, the second controlling loop, also phase-locking, and comprising the elements 3c, 11 and 12 is inhibited (by signals transmitted through the wire 10a). 70

As soon as the first loop is stabilised, the coincidences mentioned above no longer occur and the first loop is inhibited (field effect transistor 9 blocked), while the second is activated. 80

The first loop introduces a phase noise which is amplified to the level of the oscillator. In fact, the noise introduced by the dividers 5 and 6 and by the frequency P/n is multiplied by the high coefficient Nn in this loop. On the other hand, the second loop is able to operate at very high frequencies without introducing appreciable phase noise. Since this is the loop which is used after stabilization, the circuit is a useful one. 85

Now the comparator 11, which is normally a symmetric demodulator, converts all amplitude noise into a residual voltage when the loop is in equilibrium, which imposes a relative dephasing between F_1 and PN in order that this equilibrium can be achieved. It is in order to suppress this residual noise that another (fourth) loop (amplifier 14) is preferably provided. 90

This another loop does not hinder the functioning of the first (to this effect, the output current of the amplifier 14 is suitably limited). On the other hand, while the second loop is activated, this another loop has the effect of automatically realigning the output voltage of the comparator 11 on to an almost zero value, which practically eliminates the residual noise. 95

In fact while the second loop is operating, the transistor 9 being blocked, the condenser 13 retains the potential which it had taken during the operation of the first loop. At the same time, the amplifier 14 applies a positive or negative current to the condenser 13, according as to whether the output voltage of the comparator 11 is negative or positive. 100

The result is that the voltage retained in the condenser 13 is brought back to a value suitable for cancelling the effect of the output voltage of the comparator 11 on the variable capacity diode 1a. 105

Another part of the circuit of figure 1 will now be described, starting with the frequency PN generated by the oscillator 1 and picked 110

up on the output side of the separator 3a.

This part of the circuit is intended to generate a frequency F_2 which comprises, in addition to the frequency PN variable in steps of height P, a frequency increment $F_0 + \epsilon$ comprising a variable part ϵ and, possibly, a fixed part F_0 .

The simplest known method of obtaining such a frequency consists of applying the frequencies NP and $F_0 + \epsilon$ to a modulator and picking up the subtractive beats.

A method is in fact known of generating $F_0 + \epsilon$ by means of a classical iterative chain of frequency synthesis, and NP by means of a simple phase-locking loop.

However, this simple solution presents serious difficulties. In the first place, for the modulator to work under good conditions, the two carrier frequencies corresponding respectively to large variations and to small increments must be at least three times as high as the output frequency F_2 which leads to very high frequencies for these carriers if the desired frequency F_2 is high. The realisation of the programmed counter-dividers for the phase-locking loop is then very difficult; the ratio N having to be very high, the phase noise at the output of the said loop, which is multiplied by N, takes a considerable value.

A subtler known solution consists of inserting, in a classical phase-locking loop, a subtractive mixer situated between the oscillator and the programmed counter-divider and receiving on the one hand the output frequency NP of the oscillator and on the other hand the frequency increment $F_0 + \epsilon$.

This subtractive mixer produces the frequency NP, which, after division by N, is compared with a standard frequency P in the phase comparator of the loop in order to lock the oscillator on to the desired frequency $NP + F_0 + \epsilon$.

However, unless the comparator is very good, it is liable to apply to the oscillator a spectrum of extraneous frequencies of the form kP , where k is an integer.

Now the desired oscillator frequency is of the form $(N + N')P + \epsilon$, since F_0 is generally chosen to be a multiple of P. When $\epsilon = 0$ the rounded output frequency $(N + N')P$ will coincide with one of the elements of the spectrum kP , so that the oscillator will lock on to this element, distant ϵ from the desired frequency. In actual fact the phenomenon is more complex, and for symmetry reasons two extraneous elements are obtained, distant $\pm \epsilon$ from the desired frequency and straddling it. The extraneous frequencies are practically impossible to eliminate and become more obtrusive as ϵ gets smaller. (It is in fact known that a frequency modulated oscillator with a modulation frequency ϵ generates a phase noise corresponding to a dephasing which tends to infinity as ϵ tends to zero).

It has been stated already that, thanks to

the use of a triple control loop, the frequency PN available at the output of the separator 3a is uncontaminated by appreciable phase noise.

Referring back to Figure 1 a second oscillator 2 is brought into operation, by the part of the circuit described above, at a frequency adjacent to $NP + F_0 + \epsilon$, by the use, during the approach phase, of the control voltage supplied by the first loop to the first oscillator.

It can be seen that the voltage issuing from the phase comparator 7 is applied to one electrode of a variable capacity diode 2a, which is contained in the circuit of the oscillator 2, through a field effect transistor 15. This last is activated while the first loop is operative by the signal issued by the circuit 10 transmitted through an "or" gate 16. A condenser 17 retains the voltage supplied at that time by the comparator 7.

The circuit of the oscillator 2 is so designed that this voltage, applied to the diode 2a, determines an oscillation frequency in the neighbourhood of $NP + F_0 + \epsilon$. It clearly includes, for this purpose, a regulating device (not shown) which allows the increment ϵ to be varied.

It is clear that this analogical approach to the frequency is not sufficiently precise.

For this reason the output frequencies of the oscillator 2 (transmitted through a separator 19) and of the oscillator 1 (transmitted through the separator 3a) are subtracted in a mixer 18.

The resulting beat frequency $F_0 + \epsilon + \Delta$, after filtering in a band-pass filter 20, is applied to a third comparator 21, of the phase comparing type, where it is compared with a frequency $F_0 + \epsilon$, supplied by a classical iterative synthesis chain. The signal, proportional to the frequency difference Δ , which is produced by the comparator 21, is applied to the other electrode of the diode 2a, thus constituting a further (third) control loop in the circuit, which has the effect of cancelling Δ . This third loop remains active even when the first is inhibited, since it stabilises itself after the simultaneous frequency approach of the two oscillators has been effected.

The exact frequency $NP + F_0 + \epsilon$ is then collected at the output of a separator 22.

It should be stressed that, the frequency increment $F_0 + \epsilon$ being very much smaller than NP, the filtering of the beat frequency issuing from the mixer 18 presents no difficulty.

Once the approach to the frequency is completed, the second and third loops are operating, the first being inhibited.

It is preferable to suppress the residual noise in the third loop, as was done for the second, by means of an amplifier 23 with negative conductance in parallel with the variable capacity diode 2a. The amplifier 23 functions in

the same way as the amplifier 14 and constitutes a fifth control loop.

In the event of the third loop ceasing to function correctly, due to a brief interruption of the current or an extraneous voltage, it is

advisable to repeat the frequency approach procedure, then to reactivate the first loop and the frequency approach control of the oscillator 2.

For this purpose, a circuit 24 then inhibits the comparator 11, at the same time unblocking the field effect transistors 9 and 15 (by means of the "or" gate 16). This circuit may consist of a simple frequency comparator or of any device capable of detecting a beat frequency.

A signalling device 25, connected at the output side of the gate 16, indicates whether or not the circuit has reached its stable operating condition.

By way of a numerical example, to generate a frequency F_2 between 108 and 118 MHz, one could take for example $F_1 = 20$ MHz and ϵ variable by increments from 0 to 1 MHz, so that F_1 must vary from 83 to 97 MHz. If $n = 10$, the divider 6 must have a ratio programmable between the values 88 and 97, and the standard frequency P defining the step will be 1 MHz.

In general, the variable increment ϵ determined by the third loop can be varied to suit the applications envisaged, either by generating a frequency "offset", i.e. a slight shift, positive or negative, for example of ± 50 KHz, in the case of a television synthesizer, or by covering the whole of a predetermined scale to obtain a synthesizer for general use.

It is worth noting that several oscillators 2, each comprising a third and a fifth loop, can be associated with a single circuit comprising the first oscillator and the first mentioned three control loops. The frequency approach of each of the oscillators 2 would then be controlled by the comparator 7 as indicated above, but on to different frequencies $PN + F_1' + \epsilon'$, $PN + F_1'' + \epsilon''$, etc. . . ., determined by the properties of their circuits.

This method is particularly interesting in the case of a synthesizer of the "unique lateral band" type, which is required to generate pairs of frequencies.

In another connection, the circuit can be simplified for some applications by omission of certain of the loops, for example those which reduce the residual voltages fourth and fifth loops). The contingency circuit 24 could equally be omitted. However, only the circuit containing the five loops gives a completely satisfactory result in all cases.

Although in the description above F_2 has been taken as greater than F_1 , the reverse case could clearly have been considered.

In order that the circuit of figure 1 should work, it is clearly necessary that the analogical approach leads to a frequency difference be-

tween the two oscillators which is sufficiently near to the increment, so that the control by the phase-locking first loop is possible. This implies that this frequency difference must be less than the band width of the second oscillator. In certain applications this condition carries with it difficulties, or at least complications, in the realisation of the oscillators and of their analogical frequency control.

In the circuit of figure 2 these difficulties are overcome by the addition of a supplementary phase-locking, control loop effecting a complementary approach to the frequency of the second oscillator, this supplementary loop comprising a phase comparator which receives, after division of their frequency, the increment on the one hand and the frequency difference between the two oscillators resulting from the first approach on the other hand, and whose output controls the frequency of the second oscillator.

On figure 2, a certain number of the components represented in figure 1 are shown with their reference numbers augmented by 30 with respect to the corresponding numbers in figure 1.

The first oscillator 31 intended to generate the frequency $F_1 = PN$ forms part of a first, phase-locking, control loop comprising a divider 35 with fixed ratio n followed by a divider 36 with programmable ratio N and a phase comparator 37 which controls the frequency approach of the oscillator 31 by means of a field effect transistor 39 then active. The comparator 37 receives for this purpose a standard frequency P/n . The oscillator 31 thus locks rapidly on to the frequency $F_1 = PN$.

A second phase-locking control loop for the frequency of the oscillator 31 comprises a second phase comparator 41 of the sampling type which receives a spectrum of harmonics of the frequency P .

Finally, another (fourth) control loop for the frequency of the oscillator 31 comprises an amplifier 44 with negative conductance and a condenser 43.

During the approach, the signal F_1/nN is not in phase with the reference impulses P/n , so that coincidences are produced between the negative peaks of the said signals and the said impulses. The circuit 40 is then active. It activates the field effect transistor 39 to set in operation the first loop, while inhibiting the second loop (control 40a).

As soon as the first loop is stabilised (or more precisely at the end of a period predetermined by a monostable trigger circuit which forms part of the coincidence circuit 40, this period being fixed at a sufficiently high value that the stabilisation always takes place), the coincidence ceases and the field effect transistor 39 is blocked, so that the first loop is inhibited while the second and the third are activated.

A second oscillator 32 is provided to add the increment. An analogical frequency approach of the oscillator 32 is determined by the command voltage supplied at 32a by the first control loop of the oscillator 31.

The resultant frequency $NP + F_0 + \epsilon + \Delta$ is mixed, in a subtractive mixer 48, with the frequency NP of the oscillator 31, and the beat frequency $F_0 + \epsilon + \Delta$ is applied, after filtering in a band-pass filter 50, to a phase comparator 51 where it is compared with a frequency $F_0 + \epsilon$ supplied by a classical iterative synthesis chain. The beat frequency, proportional to the difference in the frequencies (or the voltage proportional to the phase), issuing from the comparator 51, is applied at 32b to a frequency control device for the oscillator 32, thus providing a further (third) control loop for the frequency of the latter.

A fifth loop is comprised, as in figure 1, of an amplifier 53 with negative conductance and a condenser 47.

In order that the analogical approach will permit, in every case, the locking-on of the oscillator 32 (taking account of its bandwidth), the frequencies presented at the two inputs of the phase comparator 51 are divided by a fixed ratio p (dividers 54 and 55), and the resultant frequencies $(F_0 + \epsilon)/p$ and $(F_0 + \epsilon + \Delta)/p$ are compared in a phase comparator 56. The output of the comparator 56, proportional to Δ/p , supplies a supplementary frequency approach to the oscillator 32. It is applied at 32c through a field effect transistor 58. This last is controlled by a coincidence circuit 57, itself controlled by the signals issuing from the dividers 54 and 55. If the spread Δ is relatively small, the third loop 32, 48, 50, 51, 32b remains active and stabilises itself. It thus takes in hand, with the fifth integral loop 53, 47, the fine control of the frequency of the oscillator 32. The supplementary approach loop is not used in this case, since no coincidences occur between the signals issuing from the dividers 54 and 55, and the field effect transistor 58 is consequently blocked.

In the case where, on the contrary, the spread Δ is too great for the third loop 32b to be able to take on directly the fine control of the oscillator 32 (which could happen for example if the increment is large, or with a change of code in the programmed divider 36), the coincidence circuit 57 unblocks, for a time predetermined by a monostable trigger circuit, the field effect transistor 58, which activates the supplementary approach loop. The latter works on a spread Δ/p , and hence permits the locking of the oscillator 32. Once this locking is achieved the supplementary approach loop is inhibited (58 being blocked) and the third and fifth loops come into action as in the case of figure 1. This circuit thus permits the realisation of larger increments $F_0 + \epsilon$ than were possible with the circuit of

figure 1. The output frequency of the circuit is taken off at 52.

In the simplified circuit of figure 3, the three control loops of the oscillator 31 are identical with those of figure 2: the chain line 59 is intended to represent all the components contained in the rectangle 59 of figure 2. The analogical frequency approach of the oscillator 32 is effected in the same way as in the circuit of figure 2 (control 32a). On the other hand, the loops 32b and 32c of figure 2 are replaced by a single loop comprising the subtractive mixer 48, the filter 50, two fixed frequency dividers 60, 62 (optional), a "phase-frequency" digital comparator 61 and an integrator circuit comprising a resistance 63 and an operational amplifier 64 with an appropriate impedance 65 (of type RC) across its terminals. The supplementary approach loop 32a is retained. The "phase-frequency" loop ends at a frequency control entry 32d to the oscillator 32. The impedance 65 is chosen so that the control loop thus constituted is of the third or fourth order (at the same time proportional and integral).

It is well known that the "phase-frequency" digital comparator supplies an output voltage in saw-tooth form, positive or negative according to the sign of the difference between the two frequencies (Δ/p , p being the ratio of the dividers 60, 62) applied at its terminals. The integration of this saw-tooth voltage by the circuit 64, 65 then gives a continuous positive or negative voltage, proportional to Δ/p , and suitable for cancelling Δ/p by control of the oscillator 32. When the spread Δ/p is reduced to a simple dephasing, the comparator 61 supplies directly a continuous voltage proportional to this dephasing, whose sign depends on the sense of the dephasing. This voltage, transmitted without modification by the circuit 64, 65, control the frequency of the oscillator 32 until the dephasing is annulled. The increment is thus introduced into the circuit in a particularly simple and efficacious manner. The circuit functions correctly even for very high values of this increment (greater than the band width of the oscillator). If the increment is relatively small, the dividers 60 and 62 will be omitted.

WHAT WE CLAIM IS:—

1. A generator of electric signals having a variable frequency comprising a main frequency and an increment, the said generator comprising a first oscillator which is controllable to generate the said main frequency, a first, phase-locking, control loop for the first oscillator, said first phase-locking loop being provided with a programmable frequency divider a second, phase-locking, control loop for the first oscillator, comprising a phase comparator for receiving the output frequency of the first oscillator and harmonics of said main frequency, means for inhibiting the

- second loop while the first loop effects a numerical approach to the frequency of the first oscillator and for inhibiting the first loop, while activating the second loop, as soon as this approach is complete, a second oscillator, means for using a control voltage applied in the first loop to control the frequency of the first oscillator to impose on the second oscillator a frequency displaced from the output frequency of the first oscillator by an amount substantially equal to the increment, and a third, phase-locking control loop for the second oscillator and comprising a phase comparator for receiving the increment and the difference in the output frequencies of the two oscillators.
2. A generator according to claim 1, including a fourth control loop arranged to be activated at the same time as the second loop, using the phase comparator of the second loop and comprising an amplifier for adjusting the output voltage of the phase comparator of the second loop to zero, and a fifth control loop, functioning at the same time as the third loop, using the phase comparator of the third loop, and comprising an amplifier of the output voltage of the third loop phase comparator which is operable to adjust the said output voltage to the value zero.
3. A generator according to claim 1 or 2, wherein the first loop comprises a phase comparator and the means for inhibiting the first loop comprises a field effect transistor having a source to drain path connecting the output of the phase comparator of the first loop to a device for controlling the frequency of the first oscillator, and wherein a condenser is connected between the said field effect transistor and the said device and serves to retain the output voltage of the said phase comparator.
4. A generator according to any of claims 1 to 3, including means for detecting the presence of a beat frequency at the input terminals of the phase comparator of the third loop, and for activating the first loop in the presence of such a beat frequency.
5. A generator according to any of claims 1 to 4, including at least one supplementary oscillator, connected in the same way as the second oscillator, but generating a variable frequency having the same main frequency and a different increment.
6. A generator according to claim 1, comprising a control loop for the frequency of the second oscillator, the said control loop comprising a phase comparator for receiving the increment and the difference between the output frequencies of the two oscillators, said control loop including means effecting a division, in a fixed ratio, of the said increment and the said difference, so as to adjust their difference to a value which will enable the locking of the second oscillator to be achieved.
7. A generator according to claim 6, wherein the control loop for the frequency of the second oscillator comprises a "phase-frequency" digital comparator, followed by an integrator circuit.
8. A generator according to claim 6, wherein the control loop for the frequency of the second oscillator comprises a phase comparator fed by two dividers which effect respectively the division of the frequencies of the increment and of the difference, and is rendered inoperative as soon as the locking of the second oscillator is effected, another control loop without frequency division then taking over.
9. A generator of electric signals substantially as hereinbefore described with reference to Figure 1 of the accompanying drawings.
10. A generator of electric signals substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.
11. A generator of electric signals substantially as hereinbefore described with reference to Figure 2 as modified by Figure 3 of the accompanying drawings.
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FIG. 1



